

PROFILE

Name	Dr. Karabi Baruah
Position & Affiliation	Assistant Professor, Department of ECE
Areas of Interest	Semiconductor Device simulation, modeling and application; VLSI
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Professional Webpage (if any)	

Educational Qualifications:

Ph.D.	NIT Silchar	India	2023
M.Tech	Tezpur University	India	2016
B.E.	Dibrugarh University	India	2013

Areas of Research: Simulation and modeling of Low-Power Semiconductor Devices and Circuits; Semiconductor Device Physics; Emerging Device Applications in Next-Generation Biosensors.

Brief Profile:

Dr. K. Baruah currently serves as an Assistant Professor in the Department of Electronics and Communication Engineering at Cambridge Institute of Technology, K R Puram, Bengaluru with specialization in semiconductor devices, microelectronics, and VLSI. She obtained her Ph.D. in Semiconductor Device Engineering from National Institute of Technology Silchar (NIT Silchar), focusing on modeling and simulation of advanced Tunnel field-effect transistors. She also holds an M.Tech in Electronics Design and Technology from Tezpur University with distinction, and a B.E. in Electronics and Telecommunication Engineering from Dibrugarh University. She has previously served as an Assistant Professor at CMR University, Lakeside campus, Bengaluru, and has academic experience as a Research Scholar, Teaching Assistant, and Faculty (Temporary) at NIT Silchar.

Her research interests include modeling and simulation of emerging semiconductor devices, microelectronics, AI-assisted transistor design, and transistor based biosensing applications. She has published several research articles in reputed international journals, along with contributions to international conferences and book chapters. She is proficient in tools such as Sentaurus TCAD, Cadence Virtuoso, LT-Spice, Tanner EDA, Multisim, Xilinx, Arduino IDE, and Keil, and has programming expertise in C, Verilog HDL, and MATLAB.

In addition to her academic and research contributions, Dr. Baruah is actively involved in organizing FDPs, short-term training programs, expert lectures, and technical events, and is a member of Indian Society for Technical Education. She also serves as a reviewer for reputed journals, including Scientific Reports and IEEE-sponsored conferences; her achievements include qualifying GATE, earning NPTEL certifications, and receiving recognition for research contributions. She is committed to advancing semiconductor research and delivering high-quality, engineering education.

Awards/ Achievements/ Academic Contributions:

1. Qualified the GATE 2014 examination conducted by Indian Institute of Technology Kharagpur.
2. Successfully completed NPTEL certifications in “Hardware Modeling using Verilog” (July–September 2025) and “Embedded Systems Design with ARM” (January–March 2025), offered by the Ministry of Education, Government of India.
3. District-Level Kabaddi Champion under the All Assam Kabaddi Association.
4. Coordinated and organized the Online STTP on “Cutting-Edge Technologies, Innovations & Applications” (11–15 March 2024) at CMR University.
5. Coordinated the STTP on “The Future of Wireless: 6G and Emerging Technologies” (15–19 April 2025) at CMR University.
6. Organized a technical session on “Antenna Design for Wireless Communication” (21 March 2025).
7. Conducted and coordinated the Arduino Expo (5 May 2025) at CMR University.
8. Coordinated the Intellectual Property Awareness Program under the National Intellectual Property Awareness Mission at the School of Engineering and Technology, CMR University (18 February 2026).
9. Completed multiple FDPs, STTPs, workshops, and certifications, including AICTE ATAL programs and NPTEL certifications.

Courses Taught: Fundamental of electronics, Digital electronics, Digital system design using verilog HDL, Control system, Embedded system, Low power VLSI, Digital VLSI design, IOT,

Publications:

Journals	[1] K. Baruah, S. M. BujarBaruah and S. Baishya, “Performance improvement of SOI Tunnel-FET using pure boron and Ge pocket layer,” Microelectronics Journal, 2024. [2] K. Baruah, B. Bhowmick and S. Baishya, “An Analytical Approach to Study the Impact of Traps on Ge- Source Double Gate PNP TFET,” IETE Journal of Research, 2023. [3] K. Baruah and S. Baishya, “Investigation of Electrical Parameters and Temperature Analysis of a Dual-Metal DG PNP TFET with Extended Source,” Engineering Research Express, Vol. 5, no. 2, 2023. [4] K. Baruah and S. Baishya, “Numerical assessment of dielectrically-modulated short-double-gate PNP TFET-based label-free biosensor”, Microelectronics Journal, vol. 133, p.105717, 2023. [5] K. Baruah, R. G. Debnath, and S. Baishya, “Technology computer-aided design simulation of G e-source double-gate S i-tunnel Field Effect Transistor: Radio frequency and linearity analysis”, International Journal
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	of RF and Microwave Computer-Aided Engineering, p.e23316, 2022. [6] K. Baruah, and S. Baishya, “Electrical noise in Ge-source double-gate PNP tunnel field effect transistor”, Indian Journal of Physics, pp.1-13, 2022. [7] K. Baruah, R. Das, and S. Baishya, “Impact of trap charge and temperature on DC and Analog/RF performances of heterostructure overlapped PNP tunnel FET”, Applied Physics A, vol. 126, no. 11, pp.1-12, 2020. [8] R. G. Debnath, K. Baruah, and S. Baishya, “DC and analog/RF performance analysis of gate extended U- shaped channel tunnel field effect transistor”, Microsystem Technologies, vol. 26, no. 9, pp.2793-2799, 2020.
Conferences	[1] K. Baruah, and S. Baishya, “Performance Evaluation of Double Gate PNP TFET and Extended-Source Double Gate PNP TFET as Label-Free Biosensor”, In Proc. of the International Conference on Electrical, Computer, Communications and Mechatronics Engineering (ICECCME), 16-18 November 2022, Maldives, IEEE (pp. 1716-1721). [2] K. Baruah, R. G. Debnath, and S. Baishya, “Study of Noise Behavior of Heterojunction Double-Gate PNP TFET for Different Parameter Variations”, In Micro and Nanoelectronics Devices, Circuits and Systems (MNDSCS) (pp. 91-97). Springer, Singapore, 2022. [3] K. Baruah, and S. Baishya, “Delta-Doped Layer-Based Hetero-Structure DG-PNP-TFET: Electrical Property and Temperature Dependence”, In Advances in Communication, Devices and Networking (ICCDN) (pp. 17-25). Springer, 2022. [4] K. Baruah, and S. Baishya, “Performance Assessment of Ge-Source Double-Gate PNP TFET Based Biosensor”, In 2022 IEEE Region 10 Symposium (TENSYP) (pp. 1-6). IEEE, 2022. [5] K. Baruah, R. Pandey, U. Chakraborty, and S. Baishya, “Optimization of Electrical Parameters in Dual Dielectric Spacer Overlapped DG Tunnel FET”, In 2020 National Conference on Emerging Trends on Sustainable Technology and Engineering Applications (NCETSTEA) (pp. 1-6). IEEE, 2020.
Book chapter	[1] K. Baruah, and P. Gupta, “A New Paradigm Shift in the Semiconductor Industry for 6G Technology: A Review”, Semiconductor Nanoscale Devices: Materials and Design Challenges, pp.286-310, 2025. [2] P. Gupta and K. Baruah, “A Perspective on Implications of 5G technology on the semiconductor industry”, Contemporary Research in Science and Technology, Notionpress. [3] K. Baruah, and S. Baishya, “Analytical Modeling of Surface Potential of a Double-Gate Heterostructure PNP Tunnel FET”, Emerging Low-Power Semiconductor Devices, pages 69-77, CRC press, 2022.

