

PROFILE

<u>Name</u>	<u>Dr. Jaya Chandwani</u>
<u>Position & Affiliation</u>	<u>Assistant Professor, Department of ECE</u>
<u>Areas of Interest</u>	<u>VLSI, MEMS</u>
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<u>Professional Webpage (if any)</u>	

Educational Qualifications:		
Ph.D	Visvesvaraya National Institute of Technology, Nagpur	2021
M.Tech	Government College of Engineering, Amravati	2013
B.Tech	Dr. Babasaheb Ambedkar Technology University, Lonere	2004
Areas of Research:		
VLSI, MEMS, IoT		
Brief Profile: (write about yourself)		
Dr. Jaya Chandwani earned her Bachelor of Technology in Electronics and Telecommunication from Dr. Babasaheb Ambedkar Technological University, Lonere, in 2011. She completed her M.Tech at Government College of Engineering, Amravati, in 2013, and obtained her Ph.D. from the Centre for VLSI and Nanotechnology at Visvesvaraya National Institute of Technology, Nagpur, in 2021. Dr. Jaya's doctoral research, supervised by Prof. Raghavendra Deshmukh, focused on the optimization of wideband piezoelectric vibration energy harvesters. Following the completion of her Ph.D., she worked as an SOC Design Engineer under the SMDP program, sponsored by the Ministry of Electronics and Information Technology (MeitY), Government of India, at Visvesvaraya National Institute of Technology, Nagpur, from August 2020 to November 2021. She oversaw the backend flow of ASIC design from RTL to GDSII, which included tasks such as floor-planning, power-planning, placement, clock tree synthesis, routing, static timing analysis, physical verification, parasitic extraction, and sign-off. The tools used for this work were Cadence Genus, Innovus, Virtuoso, Synopsys Primetime, and Mentor Graphics Calibre. She managed the tapeout of the EDU150-0 (80LQFN) at the 180nm technology node, which included 7 macros, approximately 2.4 million instances, a 1 GHz frequency, and a square shape. The floorplan was created by analyzing the data flow diagram and grouping the macros accordingly. After completing the project, Dr. Jaya joined Ramdeobaba College of Engineering and Management in Nagpur as an Assistant Professor (December 2021 - December 2022). She taught subjects such as Principles of Programming with C, IoT, Embedded Systems, and Digital Design to undergraduate students, while also handling the responsibilities of academic coordinator. She then moved to MVJ College of Engineering (April 2023 - June 2024) as an Assistant Professor, where she taught subjects including C Programming, Digital Design, Python Programming, and Embedded Systems. Dr. Jaya has published five SCI and two Scopus-indexed papers in international journals. She has also completed two NPTEL courses and several Faculty Development Programs. Her research focuses on designing,		

developing, and integrating MEMS-based energy harvesting systems, sensors, and actuators for sustainable technologies, addressing the growing need for autonomous, self-powered devices in fields such as environmental monitoring, healthcare, and IoT applications.

Awards/Achievements/Others:

1. "VLSI Design Flow: RTL to GDS" Silver Elite NPTEL online certification July-October 2024.
2. "VSD - Physical Design Flow" by Kunal Ghosh (Udemy Certification)
3. "VSD - Static Timing Analysis - I" by Kunal Ghosh (Udemy Certification)
4. "The Joy of Computing using Python" Elite NPTEL online certification July-October 2023
5. INUP Familiarization Workshop on Nanofabrication Technologies IITB, Workshop. Attended from 26th May to 28th May 2014.
6. INUP Hands-on Training Workshop on Fabrication of MEMS Sensors IITB, Workshop. Attended from 23rd Mar to 27th Mar 2015.
7. INUP Hands-on Training Workshop on Nanofabrication Tech. IITB, Workshop. Attended from 26th Mar to 30th Oct 2015.
8. Characterization of Materials (COM-2018) VNIT, Nagpur. STTP Attended from 22nd Mar to 26th Mar 2018.
9. ATAL FDP "Exploring the Technological Trends in Machine Learning and Artificial Intelligence: Need of the Hour", MVJCE, 9-10-2023 to 14-10-2023.
10. ATAL FDP "Recent Developments in high speed Semiconductor devices and next generation Flexible transparent devices: Changing the Semiconductor world", MVJCE, 16-10-2023 to 21-10-2023.
11. FDP on "Industrial Internet of Things", MVJCE, 6-6-2023 to 10-6-2023.
12. FDP on "VLSI System Design using Open Source Tools" jointly organised by Electronics and ICT Academies held from 10 - 21 February, 2025 under the "Scheme of financial assistance for setting up of Electronics and ICT Academies" of the Ministry of Electronics and Information Technology (MeitY), Government of India.

Courses Taught: Digital Electronics, Embedded Systems, IoT, Programming with C, Python Programming, Computer Organization

Publications:

1. Chandwani, J., Somkuwar, R. and Deshmukh, R., "Multi-band piezoelectric vibration energy harvester for low-frequency applications," *Microsyst Technol*, vol. 25(10), pp. 3867–3877, 2019.
2. Chandwani, J., Somkuwar, R. and Deshmukh, R., "Experimental study on band merging of non-linear multi-band piezoelectric energy harvester into single broadband using magnetic coupling," *Microsyst Technol*, vol. 26(2), pp. 657–671, 2020.
3. Somkuwar, R., Chandwani, J. and Deshmukh, R., "Bandwidth widening of piezoelectric energy harvester by free moving cylinders in liquid medium," *Microsyst Technol*, vol. 27(5), pp. 1959-1970, 2021.
4. Somkuwar, R., Chandwani, J. and Deshmukh, R., "Wideband auto-tunable vibration energy harvester using change in centre of gravity," *Microsyst Technol*, vol. 24(7), pp. 3033-3044, 2018.
5. Neelam Chandwani, Sandeep Dabhekar, Kalai Selvi, Roshan Noor Mohamed, Shahabe Saquib Abullais, Muhamood Moothedath, Ganesh Jadhav, Jaya Chandwani, Mohmed Isaqali Karobari, Ajinkya M Pawar, "Oral tissue involvement and probable factors in post-COVID-19 mucormycosis patients: a cross-sectional study", *Healthcare*, vol. 10(5), pp. 912–916, 2022.
6. Neelam D Chandwani, Neetu Maurya, Pradnya Nikhade, Jaya Chandwani, "Comparative evaluation of

antimicrobial efficacy of calcium hydroxide, triple antibiotic paste and bromelain against *Enterococcus faecalis*: An: In Vitro: study,” *Journal of Conservative Dentistry and Endodontics*, vol. 5(1), pp. 62-67, 2022.

7. Jaya Chandwani, Gauri Dhopavkar, Manjusha Tatiya, Nitin Chakole, Kulkarni Shailesh V. and Shelke Nilesh, “Security-aware analytical framework : A mathematical model and machine learning for dynamical system control in secure environments”, *Journal of Discrete Mathematical Sciences and Cryptography*, vol. 27(2-B), pp. 715-727, 2024.