PROFILE

Name	Veerappa Chikkagoudar
Position & Affiliation	Associate Professor, Department of ECE
Areas of Interest	VLSI, Digital Electronics
Email	veerappa.ece@cambridge.edu.in
LinkedIn ID	https://www.linkedin.com/in/veerappa-chikkagoudar-8b8794103/
Google Scholar ID	https://scholar.google.com/citations?hl=en&user=cmzLrDgAAAAJ
Orchid ID	
Vidwan ID	https://vidwan.inflibnet.ac.in/profile/566235
Scopus ID	
Professional Webpage (if any)	

Educational Qualifications:

Ph.D	VTU(Pursing)	India	
MTec	BVBCET, Hubli, VTU	India	2006
BE	PESCE Mandya, Mysore University	India	2002

Areas of Research:

VLSI, Single electron transistor, fin field effect transistor, digital system design.

Brief Profile: (write about yourself)

A highly dedicated and committed person with 20 years of teaching experience and 2 years of Industry experience. Qualification: B.E. degree in Electronics and Communication Engineering from Mysore University and an M.Tech degree in Digital Electronics from the Visvesvaraya Technological University, and currently pursuing Ph.D. under Visvesvaraya Technological University. Associated with CiTech from July 2012 onwards.

Academic interests include Analog Circuits, Digital circuits, Fundamentals of Hardware description Language (FHDL), CMOS VLSI, Microprocessor, Microcontroller, and Embedded Systems. Doing research in the area of Digital Circuit Design in VLSI technology.

Courses Taught:

- Digital system design using Verilog.
- Advanced VLSI
- VLSI Design and Testing.
- Optical and wireless communication
- UHV-II
- Optical fiber networks
- Verilog HDL
- Digital VLSI Design (M.Tech)
- Digital Circuit and Logic Design (M.Tech)
- Digital System Design
- Fundamentals of CMOS VLSI
- Control system
- Analog electronics circuits
- Analog and mixed mode VLSI
- Microprocessors
- Computer communication networks
- Digital Logic design
- Fundamentals of HDL (Verilog and VHDL)
- Optical fiber communication
- Information theory and coding
- Basic electronics
- AEC lab
- Logic design lab
- Microprocessors lab
- CCN&DSP lab
- VLSI Lab
- HDL Lab
- Embedded C lab

Publications/Patents:

Publications	1.SRAM Cell Design Using FinFET for Low Power and Delay Veerappa Chikkagoudar, S K Fazle Umar, Sai Dhanush R N,Syed Avaiz International journal for creative research thoughts (IJCRT) 12 (5) 2024 2.A Review on Design of Low Power and High Speed ALU Using Finfet And CMOS SAI Veerappa Chikkagoudar, K N Harishankar, Parikshith K, Pavan sharma V International journal for creative research thoughts (IJCRT) 12 (5) 2024 3.Virtual telepresence robot M Lavanya, ML Vaishnavi, MR Vaishnavi, TJ Manish, V Chikkagoudar 2021

	4.FIR Filter Implementation on FPGA Vasudha R and Jayashree Rajashekar Veerappa Chikkagoudar International Journal of Engineering Research 5 (5), 992-1128 2016 5.Design and Implementation of Pentium-M Based Floswitch for Intracluster Communication Veerappa Chikkagoudar, Prof. B. L. Desai, U N Sinha. HiPC-2006
Patents	**Application no.:** 202241075152 **Status:** Published **Title:** Automatic detection and notification of potholes and humps on roads to aid drivers
Book/Book Chapters	