PROFILE

Name	Dr. GANGADHARAIAH S L
Position & Affiliation	Assistant Professor, Department of ECE
Areas of Interest	Analog VLSI ,Digital VLSI and Design Verification
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Professional Webpage (if any)	AAD-4194-2021

Educational Qualifications:

Ph.D	MSRIT,VTU	India	2024
MTech	KREC Surathkal,Mangalore University	India	2002
BE	B.E AIT Chikmagalur, Kuvempu University	India	1997

Areas of Research:

Analog VLSI ,Digital VLSI

Brief Profile: (write about yourself)

I am Dr. Gangadharaiah S L, with extensive experience in the field of VLSI signal processing and embedded systems. My research work includes the design and development of efficient VLSI architectures for LMS Adaptive Filters, utilizing Cadence EDA tools for front-end design and verification.

I have successfully led RTL design and verification for advanced 3nm technology nodes, delivering high-performance and power-efficient designs. Additionally, I have been deeply involved in RISC-V processor development for embedded applications, where I developed and verified RTL for RISC-V (STEEL) processors. These efforts included FPGA-based proof-of-concept demonstrations and ongoing ASIC implementation using

tools such as Synopsys Design Compiler, Spyglass Lint, CDC, and RDC.

Currently, I manage a team of eight engineers specializing in embedded systems, RTL design and verification, and RISC-V processor projects. My team has demonstrated expertise in both FPGA-based and ASIC-based designs for RISC-V processors. I also have hands-on experience with SPIKE and PULP RISC-V simulators, with successful demonstrations of their functionality in embedded applications.

In addition to my technical expertise, I have conducted multiple corporate training sessions and provided consultancy services for multinational corporations, helping them enhance their technical capabilities and workforce expertise.

Add about setting up labs and consultancy (if any)

Silicon Integrated Micro Systems, Bangalore (March 2003 - July 2015):
Successfully completed consultancy projects worth ₹3,00,000. The work included providing innovative solutions in VLSI design, embedded systems, and system-level integration. I was instrumental in setting up advanced laboratories, equipped with the latest tools and technologies, to support R&D activities and skill development in VLSI and embedded domains.

Knowx Innovation, Bangalore (November 2019 - April 2022):
Provided consultancy services worth ₹1,00,000, focusing on system design improvements and technology advancements. My role included offering guidance on VLSI implementation strategies, setting up training labs for hands-on learning, and enabling innovation in embedded applications.

Tiranga Aerospace, Bangalore (July 2015 - April 2022):
Executed consultancy assignments worth ₹2,00,000. My contributions involved supporting the development of aerospace systems and integrating advanced technology solutions. I also led initiatives to establish dedicated labs for prototyping and testing aerospace technologies, fostering an environment of innovation and practical experimentation.

Chip Edge Technologies (December 2023 - August 2024):
Provided consultancy services worth ₹8,00,000, contributing extensively to technology advancements, system design optimization, and professional training. My responsibilities included setting up industry-standard labs equipped with EDA tools for VLSI and embedded systems training, ensuring the infrastructure aligned with industry requirements.

SLN Technologies (December 2023 - Present):

Currently providing consultancy services worth ₹1,00,000. My role encompasses advising on technology upgrades, system design enhancements, and training program development. I am also involved in establishing modern labs for training and R&D, facilitating practical exposure and fostering innovation in VLSI and embedded systems.

In addition to these consultancy activities, I have been deeply engaged in setting up state-of-the-art laboratories that serve as hubs for cutting-edge research, training, and development. These labs are equipped with the latest hardware and software tools, enabling hands-on learning, innovation, and the practical application of advanced VLSI and embedded system designs. My consultancy efforts ensure these labs remain aligned with evolving industry standards, enhancing their impact on education and research.

Guiding students at various levels (BE, MTech and PhD)

Supervised the successful completion of 60 undergraduate (B.E.) projects and 53 postgraduate (M.Tech) projects, providing technical expertise, mentorship, and guidance in various domains of VLSI design and signal processing.

Awards/Achievements/Others: NIL

Courses Taught:

1. BASIC ELECTRONICS
2. LOGIC DESIGN
3. DIGITAL SYSTEM DESIGN USING VHDL
4. DIGITAL SYSTEM DESIGN USING VERILOG
5. CAD FOR VLSI
6. VERY LARGE SCALE INTEGRATED CIRCUIT.
7. FPGA BASED SYSTEM DESIGN
8. DIGITAL SYSTEM DESIGN
9. ANALOG ELECTRONICS
10. SOLID STATE DEVICES & TECHNOLOGY,
11. SYNTHESIS & OPTIMIZATION OF DIGITAL CIRCUITS
12. ANALOG CMOS INTEGRATED CIRCUITS
13. ADVANCES IN VLSI
14. ADVANCED DIGITAL LOGIC DESIGN
15. ADVANCED DIGITAL LOGIC VERIFICATION(SYSTEM VERILOG)
16. LOW POWER VLSI DESIGN
17. ANALOG & MIXED MODE VLSI DESIGN
18. MACRO ELECTRONICS
19. ADVANCED LOGIC SYNTHESIS
20. MICRO ELECTRONICS
21. FABRICATION TECHNOLOGY
22. ANALOG INTEGRATED CIRCUITS.
23. PYTHON
24. ARTIFICIAL INTELLIGENCE/MACHINE LEARNING
25. DISCRETE MATHEMATICAL STRUCTURES
26. COMPUTER ARCHITECTURE AND ORGANIZATION
27. C PROGRAMMING

28.DATA STRUCTURES USING C++
29.OPERATING SYSTEMS
30.COMPUTER NETWORKS
31.UVM
32.DIGITAL ELECTGRONICS AND MICROPROCESSORS

Publications/Patents:

Publications	**1. "Design of Approximate Adders for Image Processing Applications",** 4th International Conference on Recent Trends on Electronics, Information, Communication & Technology (RTEICT- 2019), May 17th - 18th 2019, Sri Venkateswara College of Engineering, Bengaluru **2. "FPGA based Constant Rotators using Combined Coefficient Selection and Shift-Add Implementation",** 4th International Conference on Recent Trends on Electronics,Information, Communication & Technology (RTEICT 2019), May 17th – 18th 2019, SVCE, Bengaluru **3. "FPGA Based Pt-LMS Adaptive Filter",** 4th International Conference on Recent Trends on Electronics,Information, Communication & Technology (RTEICT 2019), May 17th – 18th 2019, SVCE, Bengaluru **4. "FPGA Based Efficient Feed forward FFT Architecture"** 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT-2018)" , on 18th -19th May, 2018,India. **5. "FPGA based optimized LMS Adaptive Filter using Distributed Arithmetic"** 3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology (RTEICT-2018)" , on 18th -19th May, 2018,India. 6. **"Design and Simulation of Quadrature Mirror Filters-Based Channelization Architecture For Subband Coding Applications Using FPGA",** IEEE International Conference On Recent Trends In Electronics Information Communication Technology, May 19-20, 2017, India. 7. **"Design of Schmitt Trigger based low power 12T SRAM cell"**. International conference on Ubiquitous Computing (ICUC-17),Pune,Maharashtra 25th&26th June 2017. **8. "Design of low dropout voltage regulator for low power applications".**International conference on Ubiquitous Computing (ICUC-17),Pune,Maharashtra 25th&26th June 2017. 9. **"FPGA Based area optimized parallel pipelined radix-2^2 Feed forward FFT**

architecture".IEEE International Conference on Recent Trends in Electronics Information and Communication Technology, Bangalore ,20th-21stMay 2016.

10. "**Low Leakage Power binary content addressable Memory Cell ",**International Journal of Advance Research in Science & Engineering ,Vol 05,Issue No 06,June 2016.

11. "**Congestion and power aware feed through placement methodology in a channel based SOC design at 28nm",** National Conference on Recent Innovations in Science Engineering and Technology.(NCRISET- 2016),Mysore.May -2016

12. **"Verification of deadlock recovery in NOC using encoding scheme",** International Journal of Computer Science and Information Technologies, June 2016

13. "**Top-Down Integration Methodology for Clocking Blocks into High Speed Serial IO"** International Journal on Recent & Innovation Trends in Computing and communication (IJRITCC),June15.Volume 3,Issue 6.

14. "**Challenges in Modeling and Verification of Transmitter Circuits for Advanced Mobile Storage Physical layer".** International Journal on Recent & Innovation Trends in Computing and communication (IJRITCC),June15.Volume 3,Issue 6

15. **"FPGA based fixed point LMS adaptive filters"**. International Journal of Electronics and Communication Engineering & Technology,(IJECET)Volume 6, Issue 10, Oct 2015, pp. 30-42, Article ID: IJECET_06_10_004.

16. **"Hardware Efficient WiMAX Deinterleaver Capable of Address Generation for Random Interleaving Depths"**International Journal of Engineering Trends and Technology (IJETT) – Volume 10, Number 4 - Apr 2014,

17. **"Efficient Implementation of Memory Controllers and Memories in Virtual Platform"**. IEEE International Conference on Communication and Signal Processing - ,April 3-5,2014,India Adhiparasakthi Engineering College in association with IEEE.

18. **Hybrid controller design using gain scheduling approach for compressor systems" International Journal of Electrical and Computer Engineering DOI: http://doi.org/10.11591/ijece.v12i3.pp%25p**

19. **"Modeling a Fault Detection Predictor in Compressor using Machine Learning Approach based on Acoustic Sensor Data" International Journal of Advanced Computer Science and Applications January 2021, 10.14569/IJACSA.2021.0120973**

20. "**FPGA Implementation of Efficient VLSI Architecture of DLMS Adaptive Filter Algorithm" Turkish Journal of Computer and Mathematics Education, Vol.12 No.14 (2021), 478-489.**

	21. "Integrated data aggregation with fault-tolerance and lifetime energy-aware adaptive routing in coffee plantations using WSN", Indonesian Journal of Electrical Engineering and Computer Science, Vol. 24, No. 1, pp. 376-385, Oct 2021. **22. "Capacitor – Less Low Dropout Regulator for Analog sensing using 90nm Technology"** International Journal of Circuits ,Systems and Signal Processing DOI:10.46300/9106.2021.15.129 **23. "Delay-Efficient VLSI Architecture design for robust proportionate Adaptive filter"** Indonesian Journal of Electrical Engineering and Computer Science 24. **"Design and performance analysis of Anti-Surge Control mechanism for Compressor system using Neural Networks"** International Journal of Advanced Computer Science and Applications (IJACSA) January 2022 Edition (Volume 13 No 1) 25. **"Efficient Speed Optimized VLSI Implementation of Variable Step Size LMS Algorithm" Accepted** for IAES International Journal of Artificial Intelligence (IJ-AI) for possible publication **26. "Efficient VLSI Architecture Design of Proportionate-Type LMS Adaptive Filters"Indonesian Journal of Electrical Engineering and Computer Science 26(1):67 DOI:10.11591/ijeecs.v26.i1.pp67-74** **27. "Memory-Less Distributed-Arithmetic Based Optimized VLSI Architecture of LMS Adaptive Filter"** Accepted in IJECE International Journal of Electrical and Computer Engg (Q3) 28. **"Power Optimized VLSI Architecture Of Distributed Arithmetic Based Block LMS Adaptive Filter"** International Journal of Electrical and Electronics Research (IJEER) **(Q4)** https://doi.org/10.37391/ijeer.110320 **29.** "**Anomaly Detection Using Enhanced Transient Extreme Machine Learning System in Wireless Sensor Networks"** Wireless Personal Communications https://doi.org/10.1007/s11277-023-10271-0. **30.** "**An optimized VLSI Implementation of the Least Mean Square (LMS) Adaptive Filter Architecture on the Basis of distributed Arithmetic approach"** Journal of Inst.Eng.India Ser.B https://doi.org/10.1007/s40031-024-010289-9
Patents	

	NIL
Book/Book Chapters	NIL

Research and Consultancy:

Silicon Integrated Micro Systems, Bangalore (March 2003 - July 2015):

Successfully completed consultancy projects worth ₹3,00,000, delivering innovative solutions and technical expertise.

Knowx Innovation, Bangalore (November 2019 - April 2022):

Provided consultancy services worth ₹1,00,000, contributing to advancements in technology and system design.

Tiranga Aerospace, Bangalore (July 2015 - April 2022):

Executed consultancy assignments worth ₹2,00,000, supporting aerospace technology development and system integration.

Chip Edge Technologies (December 2023 to August 2024)

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SLN Technologies (December 2023 to Till Date)

Providing consultancy services worth ₹1,00,000, contributing to advancements in technology and system design and Training.